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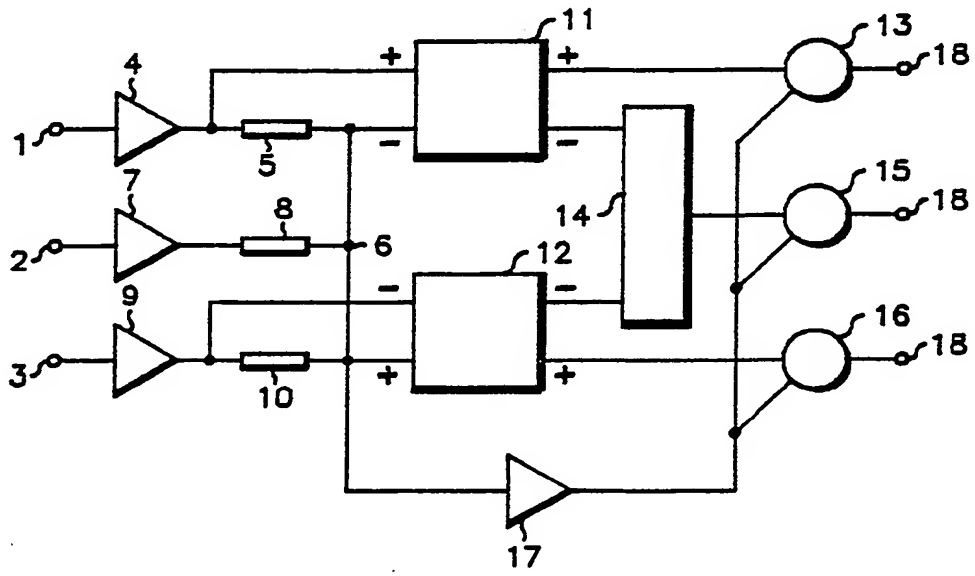

(57) Abstract

A video signal colour saturation control circuit comprising: means (1, 2, 3) for receiving RGB video signals; means (4, 7, 9, 5, 8, 10, 11, 12, 14) for deriving from the received RGB signals luminance and colour difference signals and for variably controlling the level of the colour difference signals so as to control the colour saturation; and means (13, 15, 16) for deriving from the controlled colour difference signals RGB signals which are thereby saturation controlled.

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COLOUR SATURATION CONTROL CIRCUIT

This invention relates to the processing of colour video signals and particularly, though not exclusively, to the processing of colour video signals in video monitors and television receivers.

In use of a colour video monitor the input signals may be in the form of red, green and blue (RGB) signals, e.g. from a camera. In a television receiver RGB signals are derived from a composite input signal.

It is an object of this invention to provide a saturation control circuit whereby the colour saturation of RGB signals may be varied.

In accordance with the invention a video signal colour saturation control circuit comprises:

means for receiving RGB video signals;

means for deriving from the received RGB signals luminance and colour difference signals and for variably controlling the level of the colour difference signals so as to control the colour saturation; and

means for deriving from the controlled colour difference signals RGB signals which are thereby saturation controlled.

One television receiver saturation control circuit in accordance with the invention will now be described, by way of example only, with reference to the accompanying drawing which shows a block schematic diagram of the circuit.

Referring now to the drawing, a saturation circuit includes first, second and third input nodes 1, 2 and 3 respectively.

The input node 1 is connected through a buffer amplifier 4 and through a series-connected resistor 5 to a point 6. The input node 2 is connected through a buffer amplifier 7 and a series-connected resistor 8 to the point 6. The input node 3 is connected through a buffer

amplifier 9 and a series-connected resistor 10 to the point 6.

The common point 6 is also connected to the inverting inputs of two variable gain differential amplifiers 11, 12. The output of the buffer amplifier 4 is connected to the non-inverting input of the differential amplifier 11. The output of the buffer amplifier 9 is connected to the non-inverting input of the differential amplifier 12.

The non-inverting output of the differential amplifier 11 is connected to a first input of an adder 13. The inverting outputs of the differential amplifiers 11 and 12 are connected to a resistor network 14, the output of which is connected to a first input of an adder 15. The now inverting output of the differential amplifier 12 is connected to a first input of an adder 16. Second inputs of each of the adders 13, 15, 16 are connected via a unity-gain buffer amplifier 17 to the common point 6.

The outputs of the adders 13, 15 and 16 are connected respectively to output nodes 18, 19 and 20.

In use of the circuit R, G and B signals are applied to the input nodes 1, 2 and 3 respectively. The R signal is applied directly from the output of the buffer amplifier 4 to the non-inverting input of the differential amplifier 11. The B signal is applied directly from the output of the buffer amplifier 9 to the non-inverting input of the differential amplifier 12.

The resistors 4, 8 and 10 have values of 3.33k , 1.69k and 9.1 so that the RGB signals are combined in the correct proportions at point 6 so as to produce a luminance signal Y in accordance with the well-known equation:

$$E_Y = 0.3\ E_R + 0.59\ E_G + 0.11\ E_B.$$

Thus the output of the differential amplifier 11 is a (R-Y) signal and the output of the differential amplifier

12 is a (R-Y) signal. The outputs of the differential amplifiers 11 and 12 are combined in the resistive network 14 to produce at the output of the network a (G-Y) signal in accordance with the well-known equation:

$$E_G - E_Y = - 0.51 (E_R - E_Y) - 0.186 (E_B - E_Y).$$

The (R-Y), (G-Y) and (B-Y) signals are combined in the adders 13, 15 and 16 respectively with the Y signal from the point 6 so as to produce R,G and B signals which appear at the output nodes 18, 19 and 20 respectively.

By varying the gains of the differential amplifers 11 and 12, the magnitudes of the (R-Y), (G-Y) and (B-Y) signals applied to the adders 13, 15 and 16 may be varied, thus varying the colour saturation of the colour output signals R, G and B produced at the output nodes 18, 19 and 20 respectively.

It will be understood that the gains of the differential amplifiers 11 and 12, which control saturation of the circuit, may be controlled by a microprocessor (not shown).

It will be appreciated that if desired, instead of deriving the (G-Y) signal by a resistive network using the (R-Y) and (B-Y) signals as described above, the (G-Y) signal may alternatively be derived by using a third differential amplifier having its non-inverting input connected to the output of buffer amplifer 7 and having its inverting input connected to the point 6.

It will be appreciated that the above described television receiver control circuit could also be used in any video apparatus, e.g. a video monitor.

It will also be appreciated that the above described control circuit may conveniently be incorporated in an integrated circuit.

CLAIMS

1. A video signal colour saturation control circuit comprising:

means for receiving RGB video signals;

means for deriving from the received RGB signals luminance and colour difference signals and for variably controlling the level of the colour difference signals so as to control the colour saturation; and

means for deriving from the controlled colour difference signals RGB signals which are thereby saturation controlled.

2. A circuit according to claim 1 wherein the means for deriving luminance and colour difference signals comprises buffer and combiner means for combining the received RGB in such proportions as to produce a luminance signal.

3. A circuit according to claim 2 wherein the means for deriving luminance and colour difference signals further comprises:

first differential amplifier means for receiving the luminance signal and a first one of the RGB signals and for producting a first level controlled signal representative of their difference;

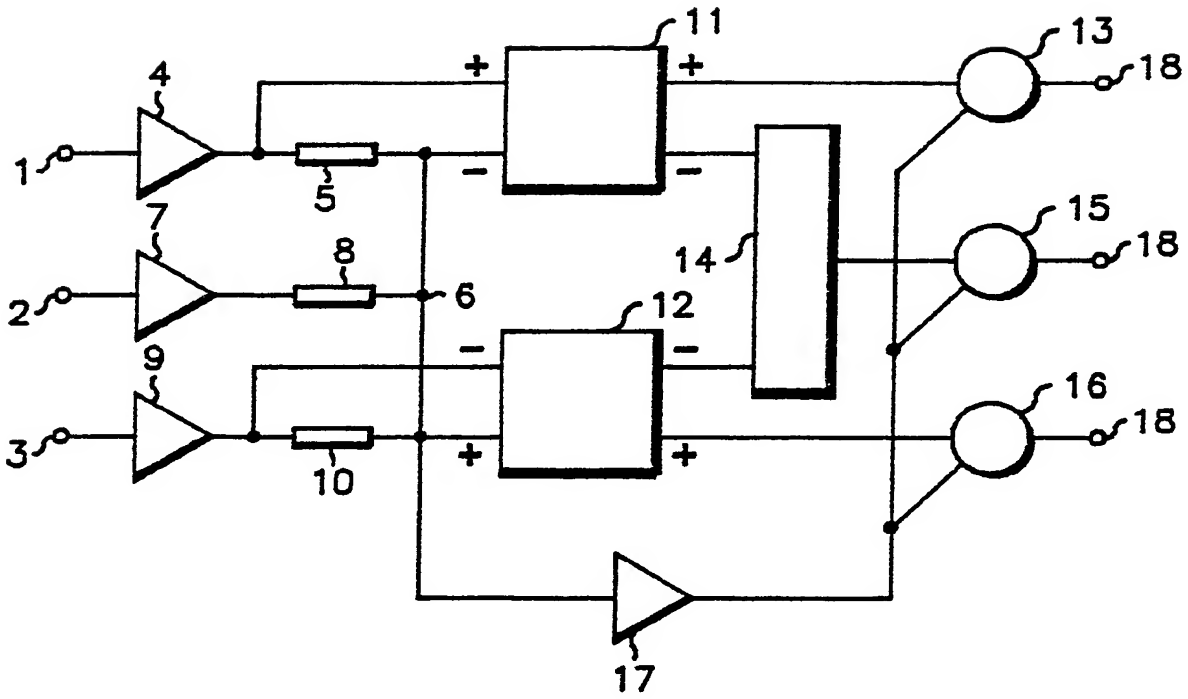
second differential amplifier means for receiving the luminance signal and a second one of the RGB signals and for producing a second level controlled signal representative of their difference;

and combiner means for combining the colour difference signals from the first and second differential amplifier means in such proportions as to produce a third level controlled colour difference signal reprsentative of the difference between the luminance signal and the third on of the RGB signals.

4. A circuit according to claim 1, 2 or 3 wherein the means for deriving comprise first, second and third summing means for receiving the luminance signal and respective ones of the level controlled colour difference signals and summing to produce saturation controlled RGB signals.

5. An integrated circuit incorporating a circuit according to any preceding claim.

6. A video display apparatus including a circuit according to any one of claims 1 to 4.



INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 85/00245

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 09 G 1/28; H 04 N 9/68

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 04 N 9/67 H 04 N 9/64 H 04 N 9/68 H 04 N 9/73

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	The Radio and Electronic Engineer, June 1966, pages 345-356, (London, GB) K.E. Johnson: "A subjective Investigation of some Errors in the Chrominance Signal Decoding Circuits of Color Television Receivers", page 346, left-hand column, line 8 - right-hand column, line 28; figures 1,3	1,2
A	FR, A, 2326098 (ROBERT BOSCH) 27 September 1976	

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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
6th September 1985	27 SEP 1985
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	G.L.M. Kruidenberg

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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/GB 85/00245 (SA 9839)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 13/09/85

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
FR-A- 2326098	22/04/77	DE-A-	2543218	07/04/77
		US-A-	4035835	12/07/77
		GB-A-	1512149	24/05/78
		CA-A-	1098614	31/03/81

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